Features

- System is Fully Qualified toBluetooth v2.1 + EDR specification
- Bluetooth v2.1 + EDR specification Operation with Full Piconet and Scatternet Support
- Low Power 1.8V operation
- 10 x 10 x 1.6mm 96-Ball LFBGA Package
- Minimum External Components
- Integrated 1.8V Regulator
- UART Port to 4Mbaud
- RF Plug-n-Go Package
- 50Ω Matched Connection to Antenna
- RoHS Compliant version available

BlueCore®4-ROM Plug-n-Go

Single Chip Bluetooth® v2.1 + EDR System

Production Information

BC41B143A

Issue 5

General Description

The BlueCore4-ROM Plug-n-Go is a single chip radio and baseband IC for Bluetooth 2.4GHz systems. It is implemented in 0.18µm CMOS technology.

BlueCore4-ROM Plug-n-Go contains 4Mb of internal ROM memory. When used with CSR Bluetooth stack, it provides a fully compliant Bluetooth v2.1 + EDR specification specification for data and voice.

The device incorporates auto-calibration and BIST routines to simplify development, type approval and production test.

Applications

- Automotive
- Industrial
- Mice
- Medical

BlueCore4-ROM Plug-n-Go has been designed to reduce the number of external components required which ensures production costs are minimised. The 0.8mm pitch BlueCore4-ROM Plug-n-Go can be used on either two or four layer PCB construction.

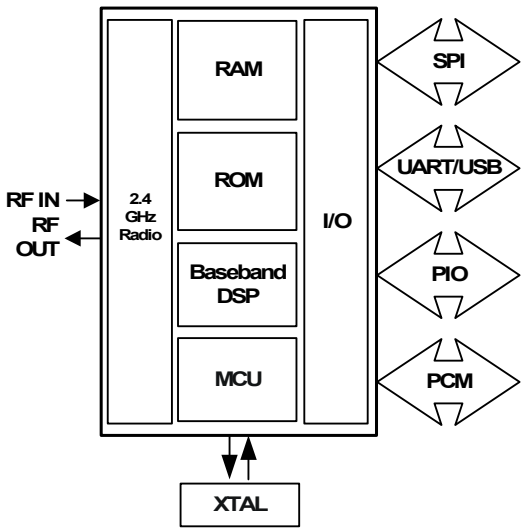

Figure: System Architecture

Document History

Revision	Date	Change Reason
Issue 1	FEB 05	Original publication of this document
2	AUG 06	Pre-production issue
3	09 JUN 09	Production version release If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.
4	10 DEC 09	Low voltage linear regulator information updated
5	15 DEC 09	Removed section 12.1 and updated section 13

Status Information

The status of this Product Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

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Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

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1 Device Details

Radio

- Direct 50Ω connection to a common TX/RX antenna
- BIST minimises production test time
- Bluetooth v2.1 + EDR specification compliant
- No external trimming is required in production
- Antenna matching and filtering within IC

Transmitter

- 6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >35dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 8MHz to 32MHz or an external clock 8MHz to 40MHz
- Accepts 7.68, 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Physical Interfaces

- Synchronous serial interface up to 4Mbps for system debugging
- UART interface with programmable baud rate up to 3Mbps with an optional bypass mode
- Full-speed USB v2.0 interface supports OHCI and UHCI host interfaces
- I^2C master compatible interface

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
- Clock request output to control external clock
- Device can run in low power modes from an external 32768Hz clock signal
- On-chip regulator, producing 1.8V output from 2.2V to 5.6V input
- Power-on-reset cell detects low supply voltage
- 8-bit ADC and DAC available to application

Baseband and Software

- 4Mb internal ROM
- 48KB internal RAM, allows full speed data transfer, mixed voice and data, and full piconet operation, including all EDR packet types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all mandatory Bluetooth v2.1 + EDR specification features including eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air
- Standard HCI over USB

Package Option

- 96-Ball 10 x 10 x 1.6mm 0.8mm pitch LFBGA

2 Device Diagram

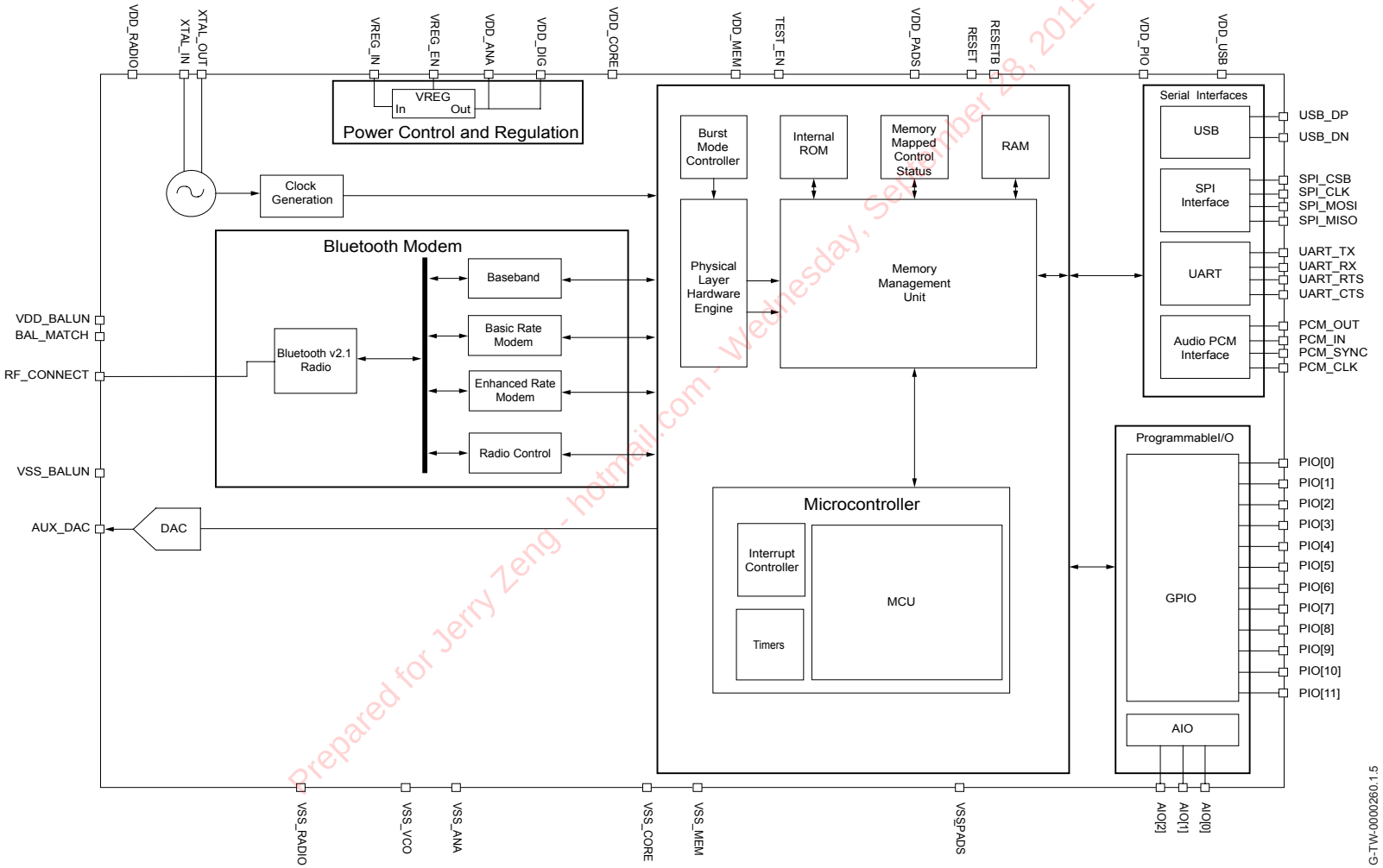


Figure 2.1: BlueCore4-ROM Plug-n-Go Device Diagram

3 Package Information

3.1 Pinout Diagram

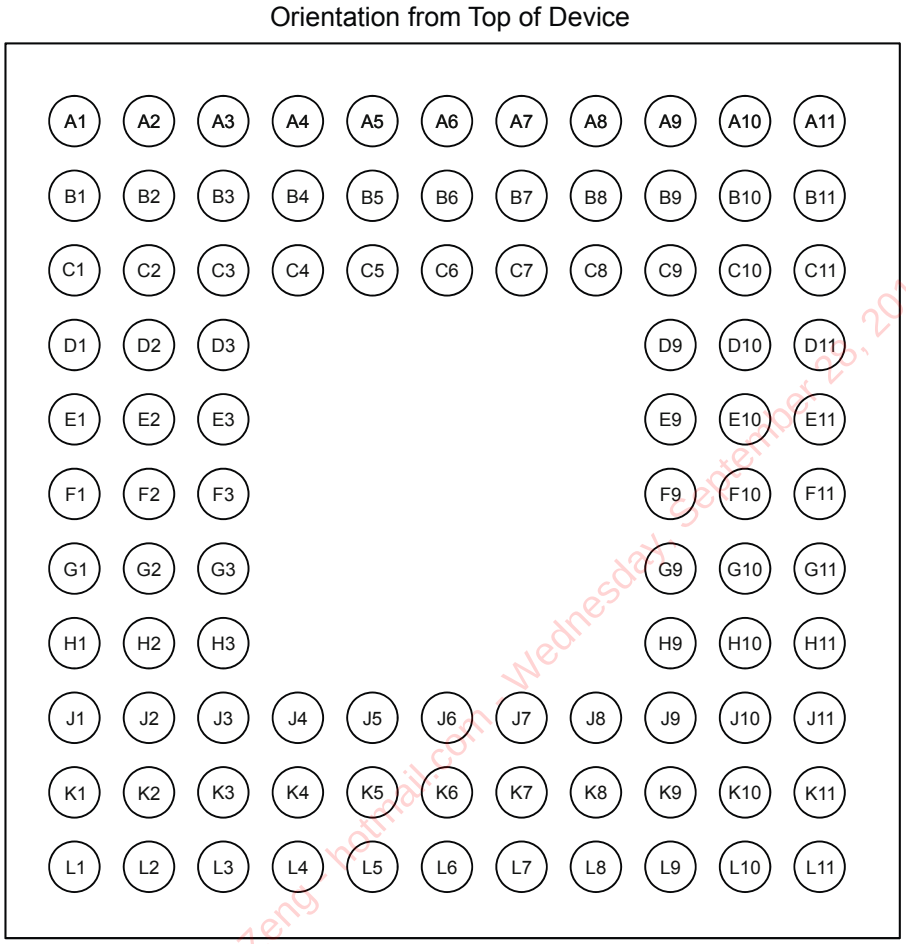


Figure 3.1: Device Pinout

3.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
BAL_MATCH	A1	Analogue	Tie to VSS_RADIO
RF_CONNECT	B1	Analogue	50 RF matched I/O
AUX_DAC	C2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L3	Analogue	For crystal or external clock input
XTAL_OUT	L4	Analogue	Drive for crystal

UART	Ball	Pad Type	Description
UART_TX	J10	Bidirectional CMOS output, tristate, with weak internal pull-up	UART data output
UART_RX	J11	CMOS input with weak internal pull-down	UART data input
UART_RTS	L11	Bidirectional CMOS output, tristate, with weak internal pull-up	UART request to send active low
UART_CTS	K11	CMOS input with weak internal pull-down	UART clear to send active low

USB	Ball	Pad Type	Description
USB_DP	L9	Bidirectional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	L8	Bidirectional	USB data minus

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G10	CMOS output, tristate, with weak internal pull-down	Synchronous data output
PCM_IN	H11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G11	Bidirectional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bidirectional with weak internal pull-down	Synchronous data clock

SPI Interface	Ball	Pad Type	Description
SPI_MISO	C11	CMOS output, tristate, with weak internal pull-down	SPI data output
SPI_MOSI	D11	CMOS input, with weak internal pull-down	SPI data input
SPI_CSB	C10	CMOS Input with weak internal pull-up	Chip select for SPI, active low
SPI_CLK	D10	CMOS Input with weak internal pull-down	SPI clock

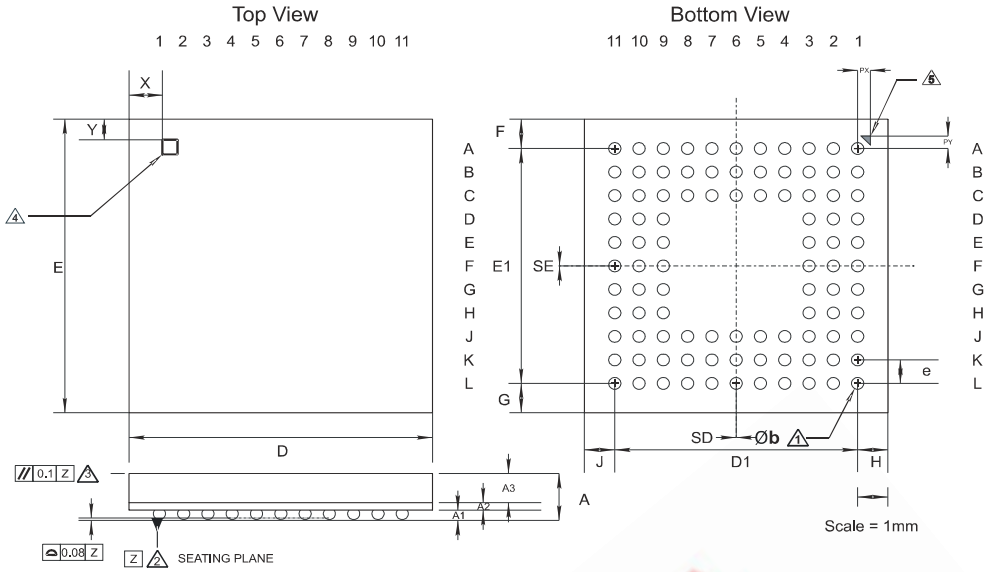
PIO Port	Ball	Pad Type	Description
PIO[0]	D3	Bidirectional with programmable strength internal pull-up/down	Programmable input/output line
PIO[1]	C4		
PIO[2]	C3		
PIO[3]	B2		
PIO[4]	H9		
PIO[5]	J8		
PIO[6]	K8		
PIO[7]	K9		
PIO[8]	B3		
PIO[9]	B4		
PIO[10]	A4		
PIO[11]	A5		
AIO[0]	K5	Bidirectional	Analogue programmable input/output line
AIO[1]	J6		
AIO[2]	K7		

Test and Debug	Ball	Pad Type	Description
RESET	F9	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESETB	G9	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
TEST_EN	E9	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	L7	Regulator Input	linear regulator voltage input
VREG_EN	J2	Digital input	Active high, regulator enable pin with internal pull-up
VDD_USB	L10	VDD	Positive supply for UART/USB and AIO ports
VDD_PIO	A3	VDD	Positive supply for PIO [3:0] and auxiliary DAC [11:8]
VDD_PADS	E11	VDD	Positive supply for all other digital Input/ Output ports, SPI/PCM ports and PIO[7:4]
VDD_DIG	L6	Regulator Output	Positive 1.8V supply output for VDD_MEM and VDD_CORE
VDD_MEM	B11, K6	VDD	Positive supply for Internal memory
VDD_CORE	F11	VDD	Positive supply for internal digital circuitry,
VDD_RADIO	E3	VDD	Positive supply for RF circuitry
VDD_ANA	L5	VDD/ Regulator output	Positive supply output for analogue circuitry and 1.8V regulated output
VDD_BALUN	F1	VDD	Positive supply for balun
VSS_PADS	A2, E10, K10	VSS	Ground connection for input/output
VSS_MEM	D9, J9	VSS	Ground connections for AIO and Extended PIO ports
VSS_CORE	F10	VSS	Ground connection for internal digital circuitry
VSS_RADIO	E2, F3, G2	VSS	Ground connections for RF circuitry
VSS_VCO	G3, H2, H3	VSS	Ground connections for VCO and Synthesiser
VSS_ANA	K4	VSS	Ground connections for analogue circuitry
VSS_BALUN	G1, J1, K1	VSS	Ground connection for balun

Unconnected Terminals	Ball	Description
NC	A6, A7, A8, A9, A10, A11, B5, B6, B7, B8, B9, B10, C1, C5, C6, C7, C8, C9, D1, D2, E1, F2, H1, J3, J4, J5, J7, K2, K3, L1, L2	Leave unconnected

3.3 Package Dimensions



Description	96-Ball Low-Profile Fine-Pitch Ball Grid Array (LFBGA)			
Size	10 x 10 x 1.6mm			
Pitch	0.8mm			
Package Ball Land	Solder mask defined. Solder mask aperture 0.3mm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A			1.6	1 Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.27	0.35	0.37	
A2		0.26		
A3		1.00		2 Datum Z is defined by the spherical crowns of the solder balls
b	0.37	0.42	0.47	
D	9.90	10.00	10.10	3 Parallelism measurement shall exclude any effect of mark on top surface of package
E	9.90	10.00	10.10	
e		0.80		
D1		8.00		4 Top-side polarity mark. The dimensions of the square polarity mark are 0.75 x 0.75mm.
E1		8.00		
F	0.950	1.000	1.050	5 Bottom-side polarity mark. The dimensions of the triangular polarity mark are 0.30 x 0.30 x 0.42mm.
G	0.950	1.000	1.050	
H	0.950	1.000	1.050	
J	0.950	1.000	1.050	
PX		0.62		
PY		0.62		
SD		0		
SE		0		
X		2.0		
Y		1.4		
JEDEC	MO-205			
Unit	mm			

Figure 3.2: 96-Ball LFBGA Package Dimensions

3.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 10 x 10 x 1.6mm LFBGA 96-Ball package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- PCB land width should be 0.2mm and PCB land length should be 0.55mm to achieve maximum reliability.
- Solder paste must be used during the assembly process.

3.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

4 Bluetooth Modem

4.1 RF Plug-n-Go

The package used on the BlueCore4-ROM Plug-n-Go device is an RF Plug-n-Go package, where the terminal RF_CONNECT forms an unbalanced ouput with a nominal 50Ω impedance. This terminal can be directly connected to an antenna requiring no impedance matching network as Figure 4.1 indicates.

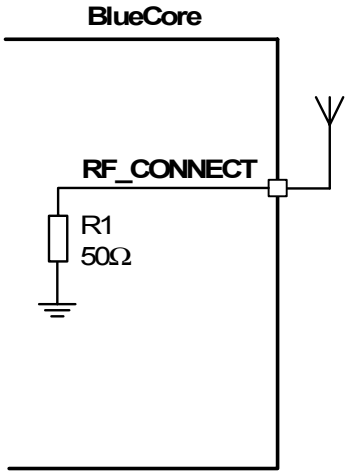


Figure 4.1: Circuit for RF_CONNECT

4.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-ROM Plug-n-Go to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

4.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

4.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

4.3 RF Transmitter

4.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

4.3.2 Power Amplifier

The internal PA has a maximum output power that allows BlueCore4-ROM Plug-n-Go to be used in Class 2 and Class 3 radios without an external RF PA.

4.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

4.5 Baseband

4.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

4.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR specification including AFH and eSCO.

4.6 Basic Rate Modem

The basic rate modem satisfies the basic data rate requirements of the Bluetooth v2.1 + EDR specification. The basic rate was the standard data rate available on the Bluetooth v1.2 specification and below, it is based on GFSK modulation scheme.

The inclusion of the basic rate modem allows BlueCore4-ROM Plug-n-Go compatibility with earlier Bluetooth products.

The basic rate modem uses the RF ports, receiver, transmitter and synthesiser, alongside the baseband components described in .

4.7 Enhanced Data Rate Modem

The EDR modem satisfies the requirements of the Bluetooth v2.1 + EDR specification. EDR has been introduced to provide 2x and 3x data rates with minimal disruption to higher layers of the Bluetooth stack. BlueCore4-ROM Plug-n-Go supports both the basic and enhanced data rates and is compliant with the Bluetooth v2.1 + EDR specification.

At the baseband level, EDR utilises both the same 1.6kHz slot rate and the 1MHz symbol rate as defined for the basic data rate. EDR differs in that each symbol in the payload portion of a packet represents 2 or 3-bits. This is achieved using two new distinct modulation schemes. Table 4.1 and Figure 4.2 summarise these. Link Establishment and management are unchanged and still use GFSK for both the header and payload portions of these packets.

The enhanced data rate modem uses the RF Ports, Receiver, Transmitter and Synthesiser, with the baseband components described in .

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Data Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 4.1: Data Rate Schemes

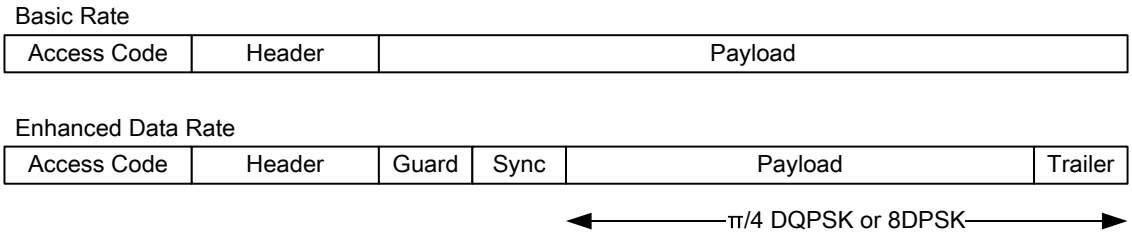


Figure 4.2: Basic Rate and Enhanced Data Rate Packet Structure

5 Clock Generation

BlueCore4-ROM Plug-n-Go requires a Bluetooth reference clock frequency of 8MHz to 40MHz from either an externally connected crystal or from an external TCXO source.

All BlueCore4-ROM Plug-n-Go internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external 8MHz to 40MHz reference clock source or an internally generated watchdog clock frequency of 1kHz.

The Bluetooth operation determines the use of the watchdog clock in low-power modes.

5.1 Clock Architecture

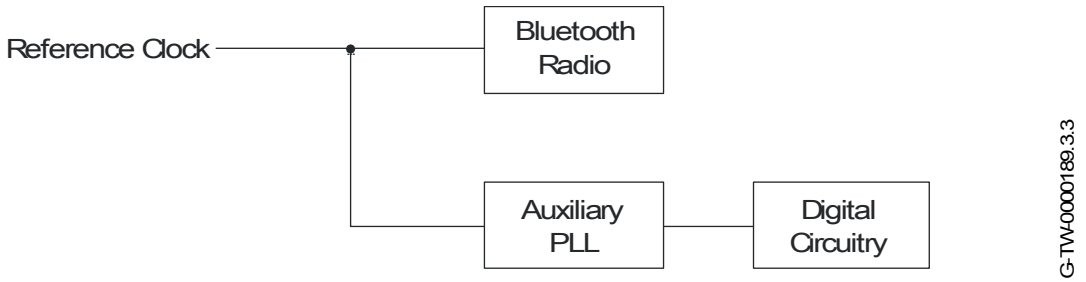


Figure 5.1: Clock Architecture

5.2 Input Frequencies and PS Key Settings

BlueCore4-ROM Plug-n-Go should be configured to operate with the chosen reference frequency. Do this by setting the PS Key PSKEY_ANA_FREQ for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore4-ROM Plug-n-Go is 16MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

The following CDMA/3G phone TCXO frequencies are also catered for: 7.68, 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. The value of the PS Key is a multiple of 1kHz, so 38.4MHz is selected by using a PS Key value of 38400.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (kHz)
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 0.25	n x 250
26.00 (default)	26000

Table 5.1: PS Key Values for CDMA/3G Phone TCXO

5.3 External Reference Clock

5.3.1 Input: XTAL_IN

The external reference clock is applied to the BlueCore4-ROM Plug-n-Go XTAL_IN input. BlueCore4-ROM Plug-n-Go is configured to accept the external reference clock at XTAL_IN by connecting XTAL_OUT to ground.

The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion. If peaks of the reference clock are either below VSS or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN.

The external reference clock signal should meet the specifications in Table 5.2.

			Min	Typ	Max	Unit
Frequency[a]			8	16	40	MHz
Duty cycle			20:80	50:50	80:20	
Edge jitter (at zero crossing)			-	-	15	ps rms
Signal level	AC coupled sinusoid		400	-	VDD_ANA[b]	mV pk-pk
	DC coupled digital	V_{IL}	-	VSS[c]	-	V
		V_{IH}	-	VDD_ANA[b] [c]	-	V

Table 5.2: External Clock Specifications

[a] The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

[b] VDD_ANA is 1.8V nominal

[c] If driven via a DC blocking capacitor max amplitude is reduced to 750mV pk-pk for non 50:50 duty cycle

5.3.2 XTAL_IN Impedance in External Mode

The impedance of XTAL_IN does not change significantly between operating modes, typically 10fF. When transitioning from deep sleep to an active state a spike of up to 1pC may be measured. For this reason CSR recommends that a buffered clock input is used.

5.3.3 Clock Start-up Delay

BlueCore4-ROM Plug-n-Go hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware, see Figure 5.2. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore4-ROM Plug-n-Go firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1ms to 31ms. Zero is the default entry for 5ms delay.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore4-ROM Plug-n-Go as low as possible. BlueCore4-ROM Plug-n-Go consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

5.3.4 Clock Timing Accuracy

As Figure 5.2 shows, the 250ppm timing accuracy on the external clock is required 2ms after the firmware begins to run. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.1 + EDR specification. Radio activity may occur after 6ms after the firmware starts. Therefore, at this point the timing accuracy of the external clock source must be within ±20ppm.

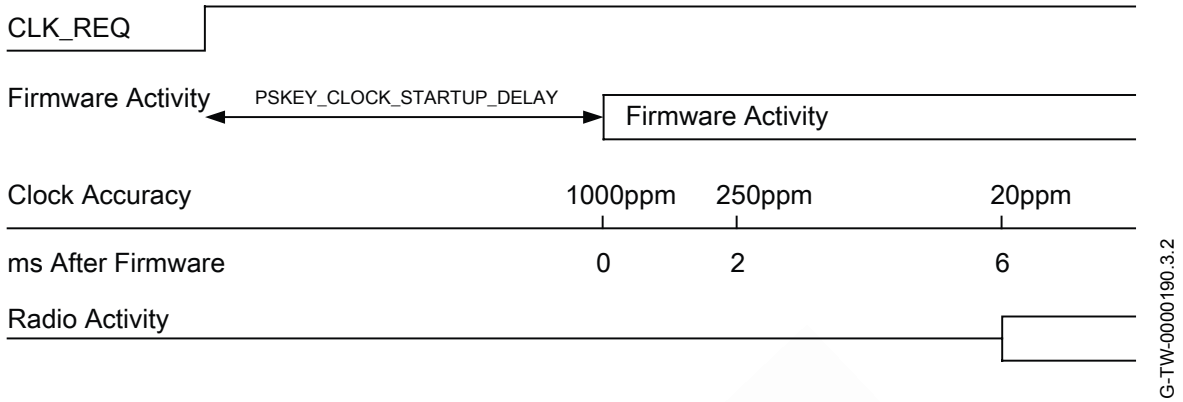


Figure 5.2: TCXO Clock Accuracy

5.3.5 External 32kHz Clock

A 32kHz clock can be applied to AIO[0] by setting DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE.

If the external clock is applied to the analogue pad AIO[0], the digital signal should be driven with a maximum 1.8V.

Note:

If the 32kHz clock is accurate and stable to within 200ppm, then further power saving features can be enabled. See the relevant software release note for more information.

5.4 Crystal Oscillator: XTAL_IN and XTAL_OUT

BlueCore4-ROM Plug-n-Go contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. The external crystal is connected to pins XTAL_IN, XTAL_OUT.

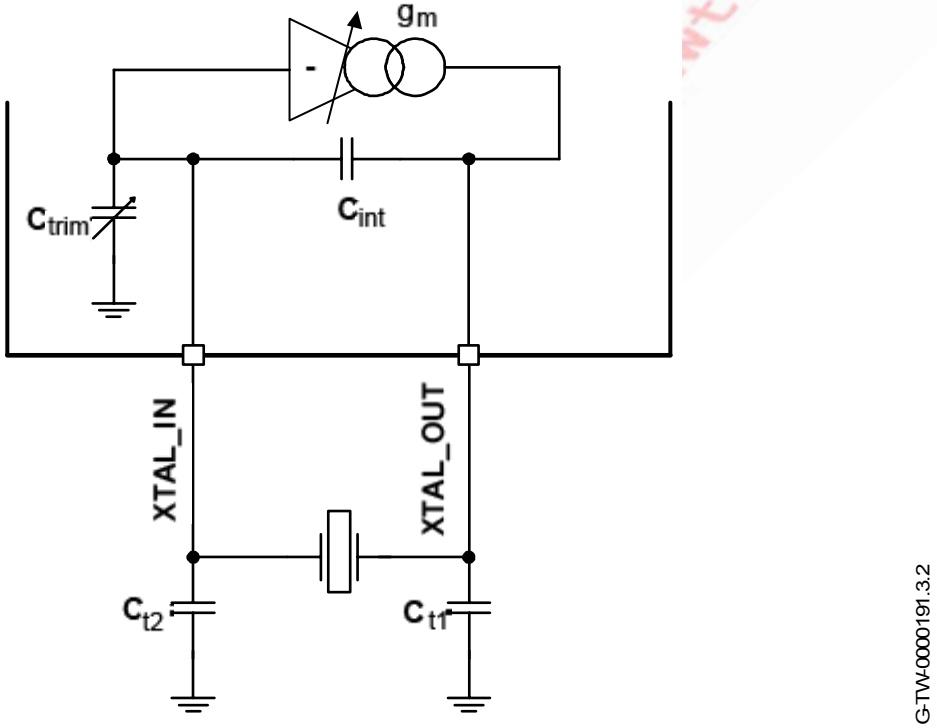
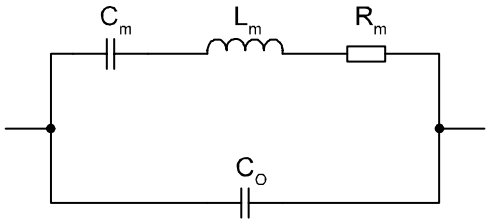


Figure 5.3: Crystal Driver Circuit

Figure 5.4 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.



G-TW-0000245.4.4

Figure 5.4: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore4-ROM Plug-n-Go contains variable internal capacitors to provide a fine trim.

Parameter	Min	Typ	Max	Unit
Frequency	8	16	32	MHz
Initial Tolerance	-	±25	-	ppm
Pullability	-	±20	-	ppm/pF

Table 5.3: Crystal Specification

The BlueCore4-ROM Plug-n-Go driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

5.4.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore4-ROM Plug-n-Go provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing and slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated with Equation 5.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})\ C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 5.1: Load Capacitance

Note:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

5.4.2 Frequency Trim

BlueCore4-ROM Plug-n-Go enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, C_{trim}. The value of C_{trim} is set by a 6-bit word in the PSKEY_ANA_FTRIM. Its value is calculated as follows:

$$C_{trim} = 125fF \times PSKEY\_ANA\_FTRIM$$

Equation 5.2: Trim Capacitance

The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of PSKEY_ANA_FTRIM.

Equation 5.3 describes the frequency trim.

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right)(\text{ppm/LSB})$$

Equation 5.3: Frequency Trim

Note:

F_x = crystal frequency

Pullability is a crystal parameter with units of ppm/pF

Total trim range is 0 to 63

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 5.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \cdot \frac{C_m}{2(C_l + C_0)^2}$$

Equation 5.4: Pullability

Note:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model), see Figure 5.4

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

5.4.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore4-ROM Plug-n-Go uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 5.5.

$$g_m > 3\,\frac{(2\pi F_x)^2\, R_m\, ((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}\,(C_{t2} + C_{trim}))}{C_{t1}\,(C_{t2} + C_{trim})}$$

Equation 5.5: Transconductance Required for Oscillation

BlueCore4-ROM Plug-n-Go guarantees a transconductance value of at least 2mA/V at maximum drive level.

Note:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

5.4.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore4-ROM Plug-n-Go crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance can be calculated for it using Equation 5.6.

$$R_{neg} > \frac{C_{t1}(C_{t2} + C_{trim})}{g_m(2\pi F_x)^2(C_0 + C_{int})((C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim}))^2}$$

Equation 5.6: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore4-ROM Plug-n-Go driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

5.4.5 Crystal PS Key Settings

The BlueCore4-ROM Plug-n-Go firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. The PSKEY_XTAL_TARGET_AMPLITUDE is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

BlueCore4-ROM Plug-n-Go should be configured to operate with the chosen reference frequency.

6 Bluetooth Stack Microcontroller

A 16-bit RISC MCU is used for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

6.1 Programmable I/O (PIO) Parallel Ports

15 lines of programmable bi-directional I/O are provided. PIO[11:8,3:0] are powered from VDD_PIO, PIO[7:4] are powered from VDD_PADS and AIO[2:0] are powered from VDD_USB.

Any of the PIO lines are configurable as button inputs or control outputs. Certain PIOs also have dedicated functions that are accessed using appropriate PS Keys. Using PSKEY_CLOCK_REQUEST_ENABLE, PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful in detecting when BlueCore4-ROM Plug-n-Go is entering or leaving deep sleep.

Note:

CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

BlueCore4-ROM Plug-n-Go has 3 general-purpose analogue interface pins, AIO[2:0], used to access internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 10-bit ADC. Signals selectable on this interface include the band gap reference voltage and a variety of clock signals: 64, 48, 32, 24, 16, 12, 8, 6 and 2MHz (output from AIO[0] only) and the XTAL and XTAL/2 clock frequency (output from AIO[0] and AIO[2]). When used with analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_ANA.

6.2 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4-ROM Plug-n-Go where either device can turn on the clock without having to wake up the other device, see Figure 6.1. PIO[3] can be used as the host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4-ROM Plug-n-Go.

Note:

To turn on the clock, the clock enable signal on PIO[3] must be high.

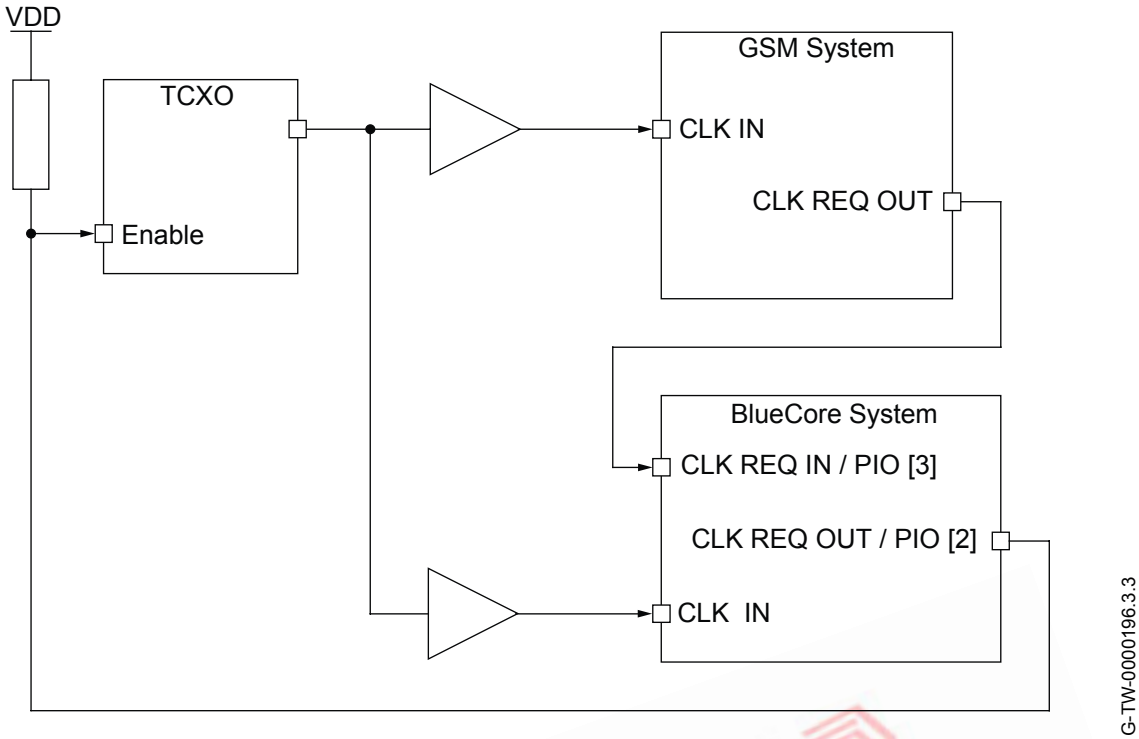


Figure 6.1: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] is tristate. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

6.3 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of WLAN coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware.

For more information see *Bluetooth and IEEE 802.11 b/g Co-existence Solutions Overview*.

7 Memory Interface and Management

7.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is transferred between BlueCore4-ROM Plug-n-Go and the air, or the host. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.2 System RAM

48KB of on-chip RAM supports the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

7.3 Internal ROM

4Mb of internal ROM is provided on the BlueCore4-ROM Plug-n-Go. This memory is provided for system firmware implementation.

8 Serial Interfaces

8.1 USB Interface

BlueCore4-ROM Plug-n-Go has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on the BlueCore4-ROM Plug-n-Go acts as a USB peripheral, responding to requests from a master host controller.

BlueCore4-ROM Plug-n-Go supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)*, available from http://www.usb.org. For more information on how to integrate the USB interface on BlueCore4-ROM Plug-n-Go see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

8.2 Programming and Debug Interface

Important Note:

The SPI is used to configure (using PS Keys) and debug the BlueCore4-ROM Plug-n-Go. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header.

CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

BlueCore4-ROM Plug-n-Go uses a 16-bit data and 16-bit address programming and debug interface. Transactions can occur when the internal processor is running or is stopped. For more information, see the *Using SPI Design Guide*.

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

8.3 UART Interface

BlueCore4-ROM Plug-n-Go has a standard UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

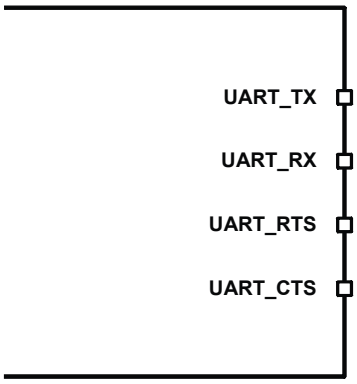


Figure 8.1: Universal Asynchronous Receiver

Figure 8.1 shows the 4 signals that implement the UART function. When BlueCore4-ROM Plug-n-Go is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, can implement RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore4-ROM Plug-n-Go firmware.

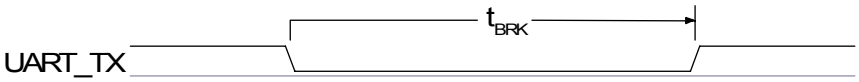
Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 8.1: Possible UART Settings

The UART interface can reset BlueCore4-ROM Plug-n-Go on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as Figure 8.2 shows. If t_{BRK} is longer than the value, defined by PSKEY_HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature allows a host to initialise the system to a known state. Also, BlueCore4-ROM Plug-n-Go can emit a break character that may be used to wake the host.



G-TW-0000250.3.2

Figure 8.2: Break Signal

Note:

Load the DFU boot loader to the Flash device before using the UART or USB interfaces. Use the SPI for this initial Flash programming procedure.

Table 8.2 shows a list of commonly used baud rates and their associated values for the PSKEY_UART_BAUDRATE. There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 8.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 8.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%
3686400	0x3afb	15099	0.00%

Table 8.2: Standard Baud Rates

8.3.1 UART Configuration While Reset is Active

The UART interface for BlueCore4-ROM Plug-n-Go is tristate while the chip is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when BlueCore4-ROM Plug-n-Go reset is de-asserted and the firmware begins to run.

8.3.2 UART Bypass Mode

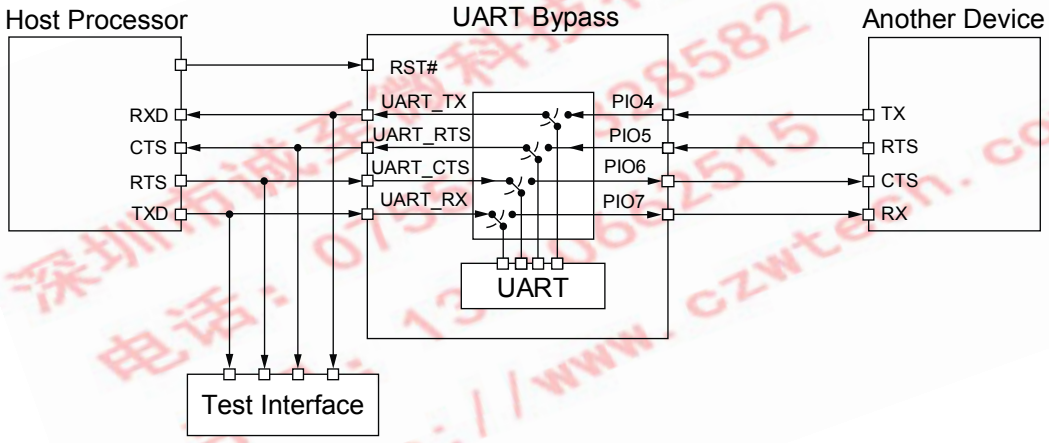


Figure 8.3: UART Bypass Architecture

Alternatively, for devices that do not tristate the UART bus, the UART bypass mode on BlueCore4-ROM Plug-n-Go can be used. The default state of BlueCore4-ROM Plug-n-Go after reset is de-asserted; this is for the host UART bus to be connected to the BlueCore4-ROM Plug-n-Go UART, thereby allowing communication to BlueCore4-ROM Plug-n-Go via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.

To apply the UART bypass mode, a BCCMD command is issued to BlueCore4-ROM Plug-n-Go. Upon this issue, it switches the bypass to PIO[7:4] as Figure 8.3 shows. When the bypass mode has been invoked, BlueCore4-ROM Plug-n-Go enters the deep sleep state indefinitely.

To re-establish communication with BlueCore4-ROM Plug-n-Go, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

Note:

When in bypass mode, the UART signal levels on the PIO are at VDD_PADS level and when not bypassed, i.e. when using the normal UART pins, the levels are at VDD_USB levels.

8.3.3 Current Consumption in UART Bypass Mode

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

8.4 Serial Peripheral Interface

The primary function of the SPI is for debug. BlueCore4-ROM Plug-n-Go uses a 16-bit data and 16-bit address SPI, where transactions may occur when the internal processor is running or is stopped. This section describes the interface considerations for connection to BlueCore4-ROM Plug-n-Go.

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

8.4.1 Instruction Cycle

The BlueCore4-ROM Plug-n-Go is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 8.3 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 8.3: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4-ROM Plug-n-Go on the rising edge of the clock line SPI_CLK. When reading, BlueCore4-ROM Plug-n-Go replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore4-ROM Plug-n-Go offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

8.4.2 Writing to the Device

To write to BlueCore4-ROM Plug-n-Go, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CS# is taken high.

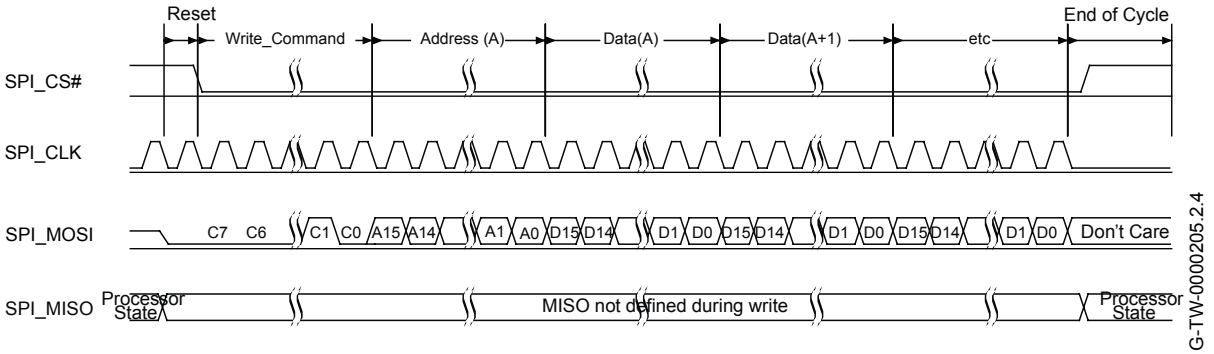


Figure 8.4: SPI Write Operation

8.4.3 Reading from the Device

Reading from BlueCore4-ROM Plug-n-Go is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore4-ROM Plug-n-Go then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CS# is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CS# is taken high.

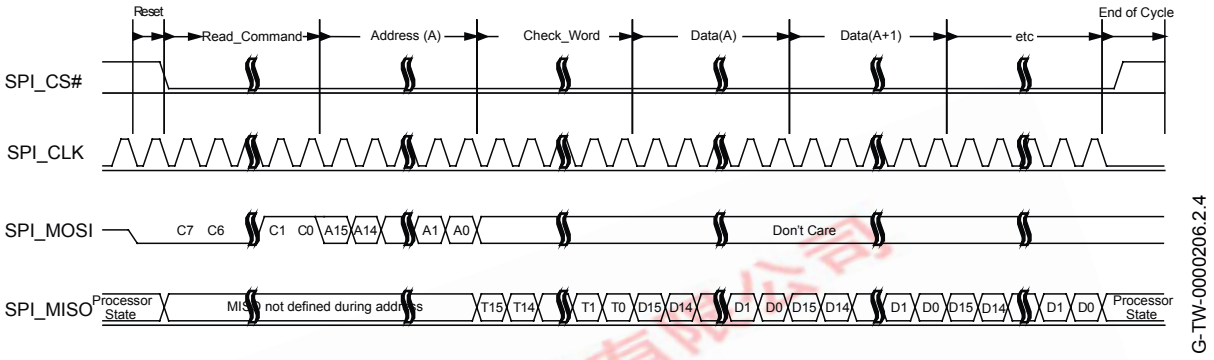


Figure 8.5: SPI Read Operation

8.4.4 Multi-slave Operation

BlueCore4-ROM Plug-n-Go should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4-ROM Plug-n-Go is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BlueCore4-ROM Plug-n-Go outputs 0 if the processor is running or 1 if it is stopped.

8.5 I²C Interface

8.5.1 Software I²C Interface

PIO[8:6] can be used to form a master I²C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix LCD, keyboard scanner or EEPROM.

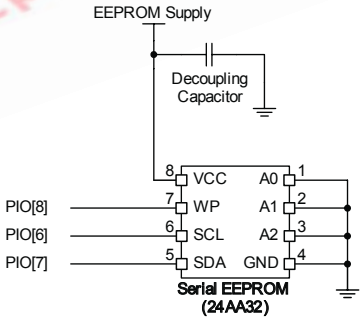


Figure 8.6: Example EEPROM Connection

8.5.2 Bit-serialiser Interface

In addition to the software I²C interface outlined in Section 8.5.1, the BlueCore4-ROM Plug-n-Go includes a configurable hardware bit-serialiser interface. Any 3 PIOs can be used as a serial master interface by configuring the hardware bit-serialiser. In the I²C master mode, the hardware bit-serialiser supports address, direction and ACK handling, but does not support multi-master I²C bus systems. I²C slave mode is also not supported.

9 Audio Interface

9.1 PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

PCM is a standard method used to digitise audio, particularly voice, for transmission over digital communication channels. Through its PCM interface, BlueCore4-ROM Plug-n-Go has hardware support for continual transmission and reception of PCM data, so reducing processor overhead. BlueCore4-ROM Plug-n-Go offers a bidirectional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore4-ROM Plug-n-Go allows the data to be sent to and received from a SCO connection.

Up to 3 SCO connections can be supported by the PCM interface at any one time.

BlueCore4-ROM Plug-n-Go can operate as the PCM interface master generating PCM_SYNC and PCM_CLK or as a PCM interface slave accepting externally generated PCM_SYNC and PCM_CLK. BlueCore4-ROM Plug-n-Go is compatible with various clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats, and can receive and transmit on any selection of 3 of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32.

9.1.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore4-ROM Plug-n-Go generates PCM_CLK and PCM_SYNC.

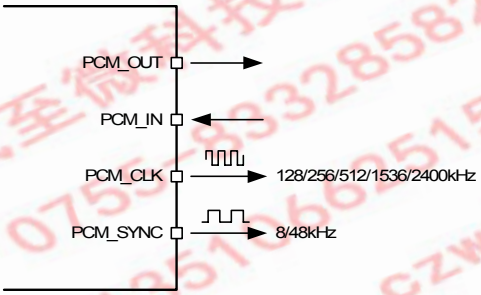


Figure 9.1: PCM Interface Master

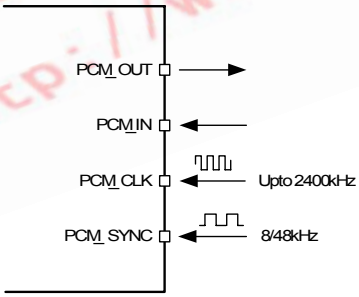


Figure 9.2: PCM Interface Slave

9.1.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-ROM Plug-n-Go is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4-ROM Plug-n-Go is configured as PCM Slave, PCM_SYNC may be from one cycle PCM_CLK to half the PCM_SYNC rate.

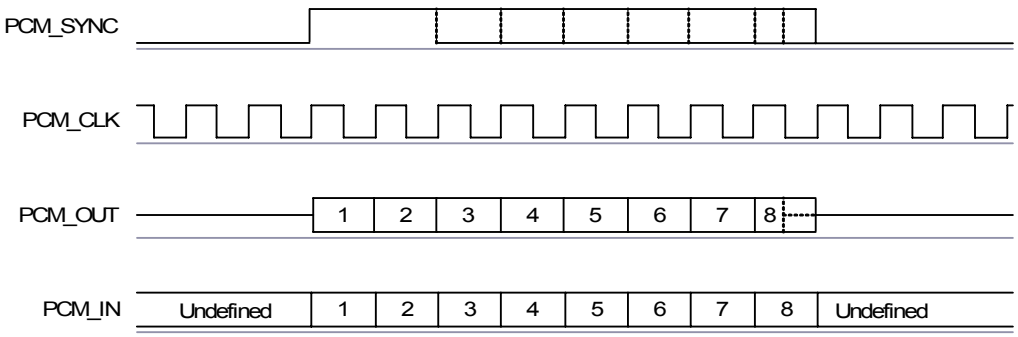


Figure 9.3: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4-ROM Plug-n-Go samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.1.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

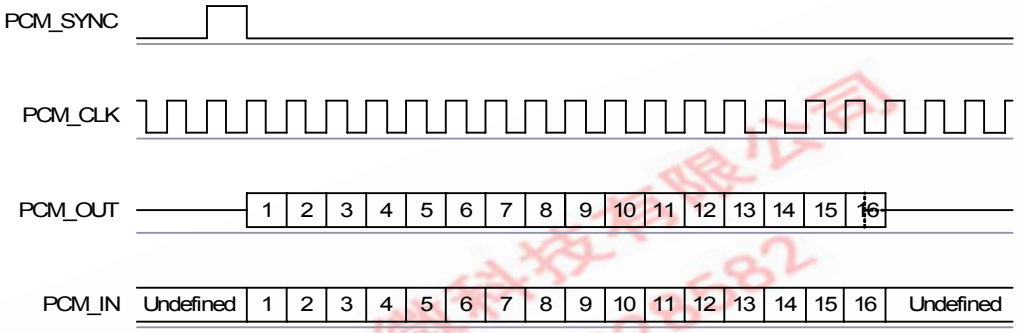


Figure 9.4: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4-ROM Plug-n-Go samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.1.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

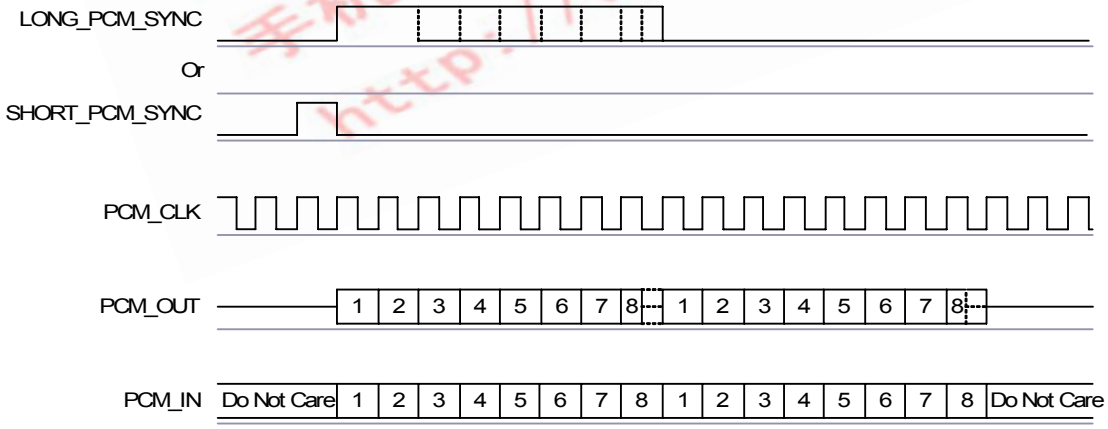


Figure 9.5: Multi-slot Operation with Two Slots and 8-bit Companded Samples

9.1.5 GCI Interface

BlueCore4-ROM Plug-n-Go is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The 2 64kbps B channels can be accessed when this mode is configured.

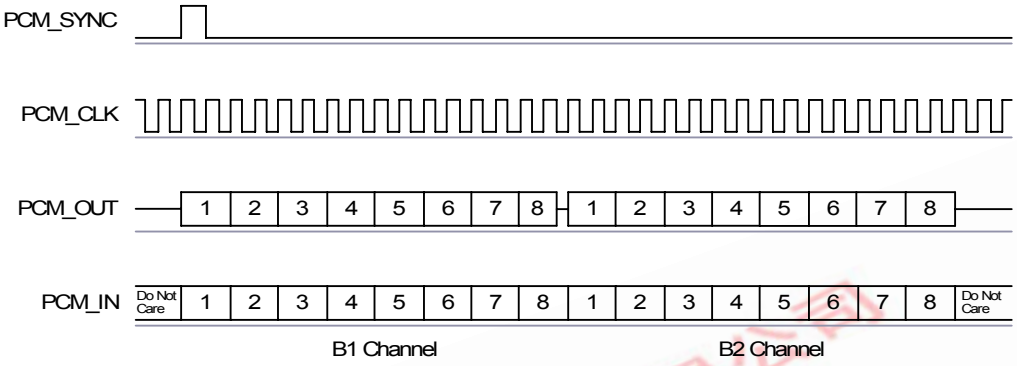


Figure 9.6: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz.

9.1.6 Slots and Sample Formats

BlueCore4-ROM Plug-n-Go can receive and transmit on any selection of the first 4 slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore4-ROM Plug-n-Go supports 13-bit linear, 16-bit linear and 8-bit µ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola codecs.

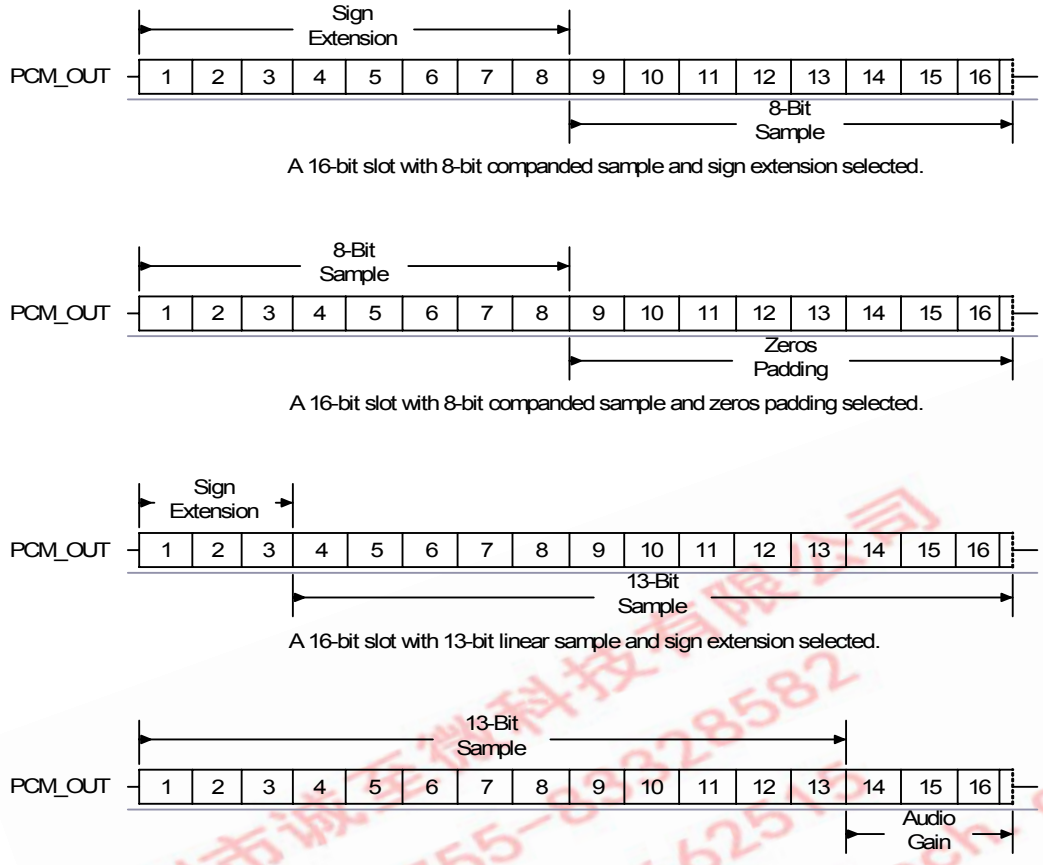


Figure 9.7: 16-Bit Slot Length and Sample Formats

9.1.7 Additional Features

BlueCore4-ROM Plug-n-Go has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some codecs use to control power down.

9.1.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 9.4.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Selection of frequency is programmable. See Table 9.3 and Section 9.1.9.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} (a)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} (a)	PCM_CLK low	4MHz DDS generation	730	-	-	ns

Symbol	Parameter		Min	Typ	Max	Unit
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 9.1: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low-power modes, when system clock speeds are reduced.

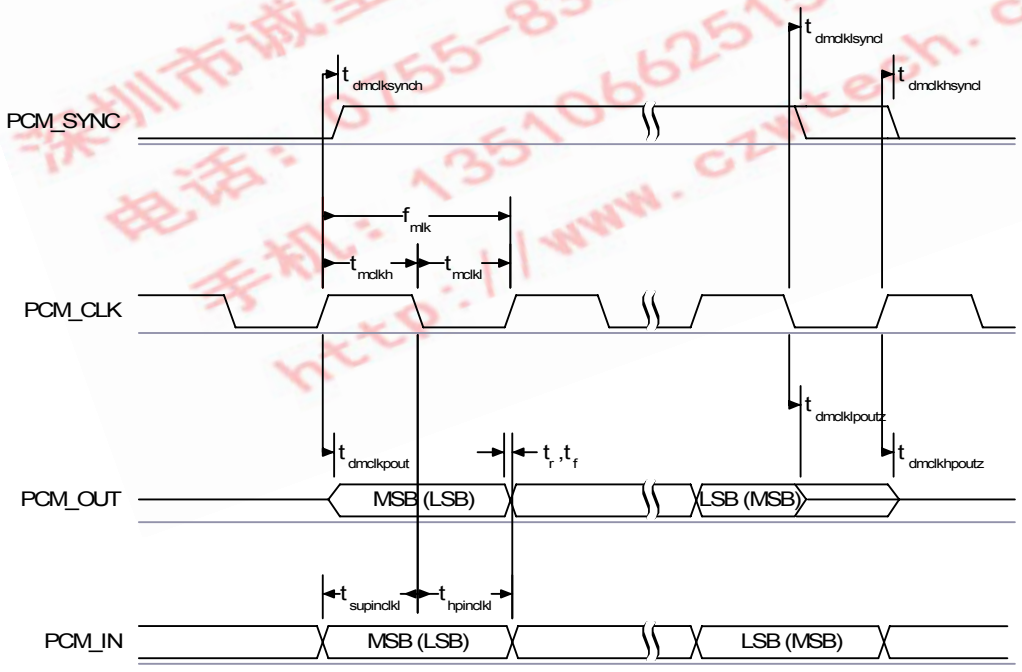


Figure 9.8: PCM Master Timing Long Frame Sync

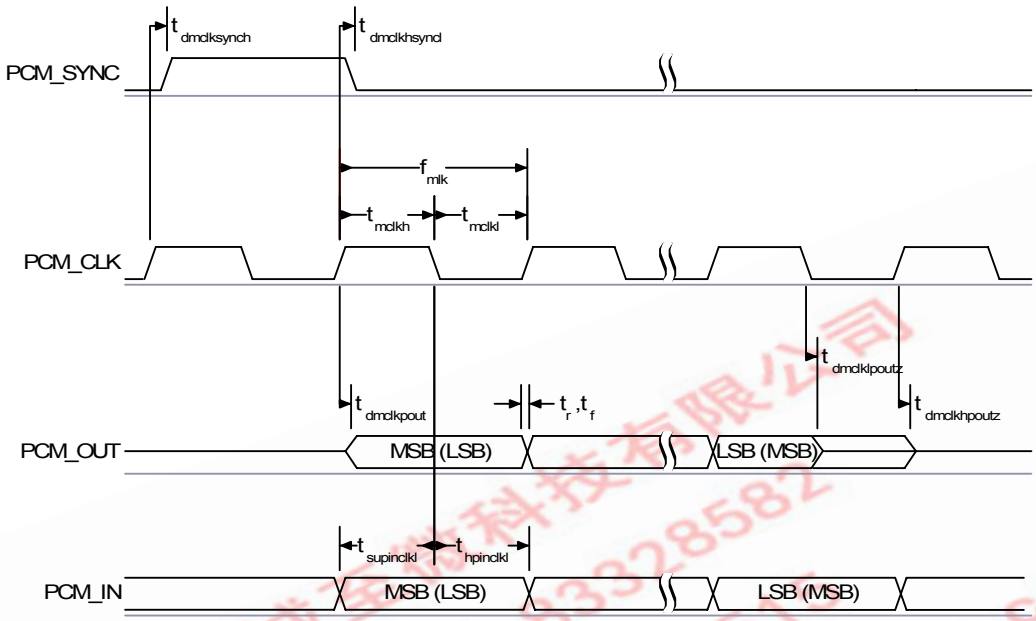


Figure 9.9: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	(a)	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	(b)	kHz
t_{sclkl}	PCM_CLK low time	80	-	-	ns
t_{sclkh}	PCM_CLK high time	80	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	20	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	20	-	-	ns

Table 9.2: PCM Slave Timing

(a) Max frequency is the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

(b) Max frequency is twice the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

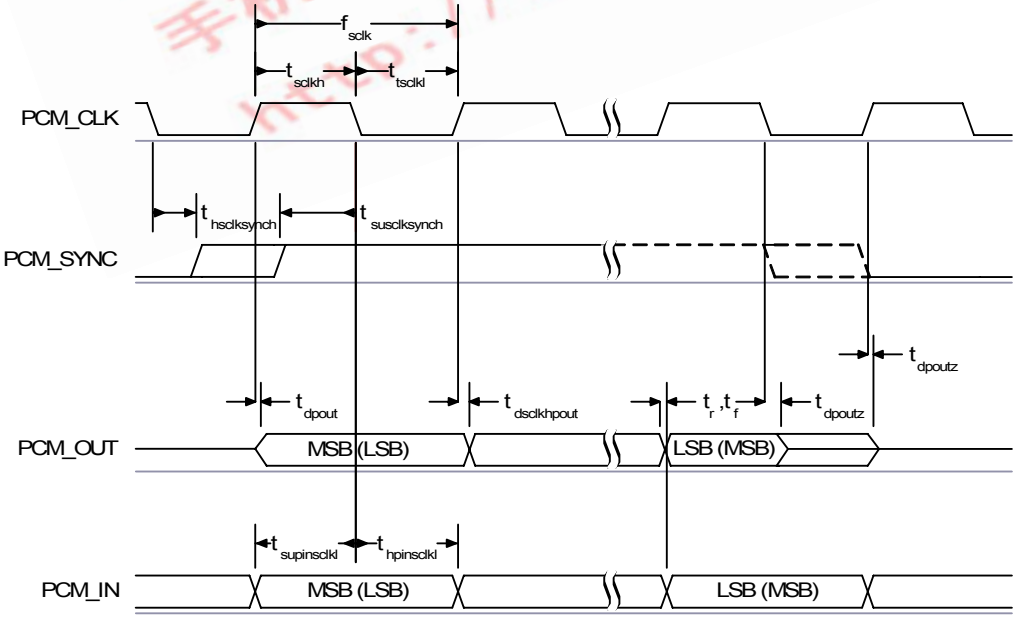


Figure 9.10: PCM Slave Timing Long Frame Sync

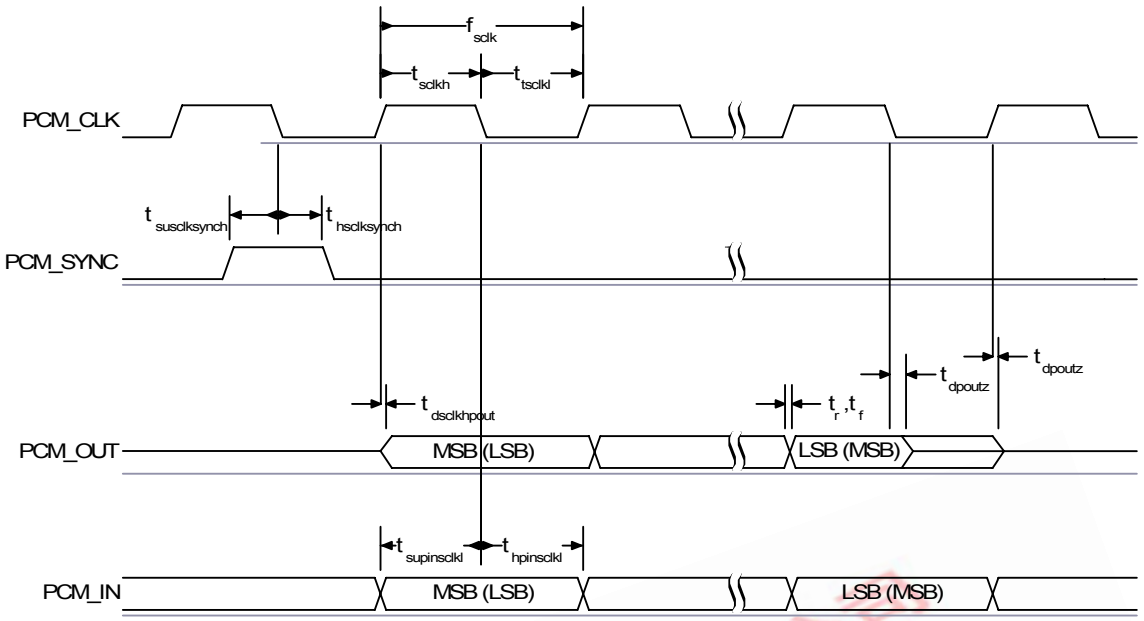


Figure 9.11: PCM Slave Timing Short Frame Sync

9.1.9 PCM_CLK and PCM_SYNC Generation

BlueCore4-ROM Plug-n-Go has 2 methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from BlueCore4-ROM Plug-n-Go internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 9.1 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 9.1: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 9.2:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 9.2: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

9.1.10 PCM Configuration

The PCM configuration is set using the PS Keys, PSKEY_PCM_CONFIG32 described in Table 9.4 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 9.3. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristate of PCM_OUT.

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 9.3: PSKEY_PCM_LOW_JITTER_CONFIG Description

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tristate PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tristate PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tristate PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC while keeping PCM_CLK running. Some codecs use this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode.
MUTE_EN	10	1 = force PCM_OUT to 0.

Name	Bit Position	Description
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16-cycle slot duration or 8 (0b11) bit sample with 8-cycle slot duration.

Table 9.4: PSKEY_PCM_CONFIG32 Description

9.2 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 9.5 lists these alternative functions. Figure 9.12 shows the timing diagram.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 9.5: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Table 9.6 describes the values for the PS Key PSKEY_DIGITAL_AUDIO_CONFIG that is used to set-up the digital audio interface. For example, to configure an I²S interface with 16-bit SD data set PSKEY_DIGITAL_AUDIO_CONFIG to 0x0406.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17-bit SD data is rounded down to 16bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16bit, 01=20bit, 10=24bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17-bit SD_IN data is rounded down to 16bits. For 1 only the most significant 16bits of data are received.

Table 9.6: PSKEY_DIGITAL_AUDIO_CONFIG

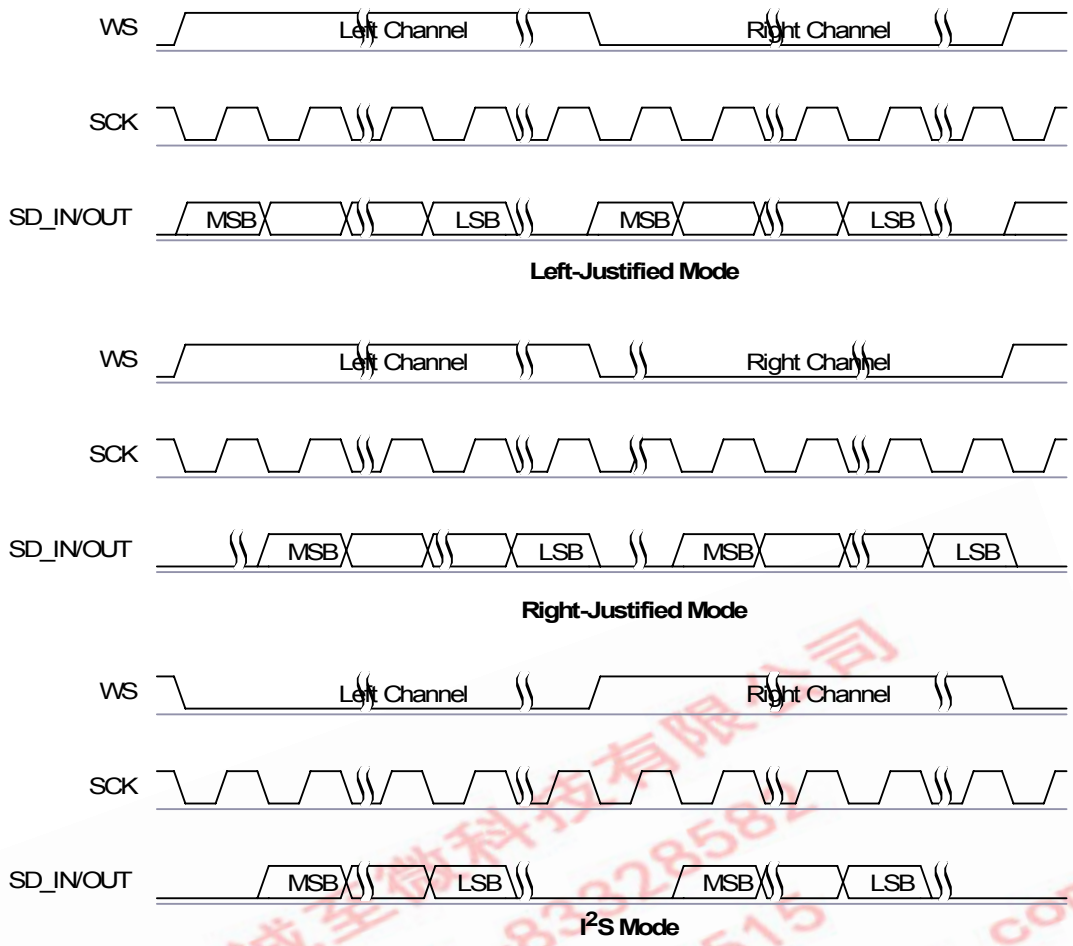


Figure 9.12: Digital Audio Interface Modes

The internal representation of audio samples within BlueCore4-ROM Plug-n-Go is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency				
-	WS Frequency				
t_{ch}	SCK high time				
t_{cl}	SCK low time				
t_{opd}	SCK to SD_OUT delay				
t_{ssu}	WS to SCK set-up time				
t_{sh}	WS to SCK hold time				
t_{isu}	SD_IN to SCK set-up time				
t_{ih}	SD_IN to SCK hold time				

Table 9.7: Digital Audio Interface Slave Timing

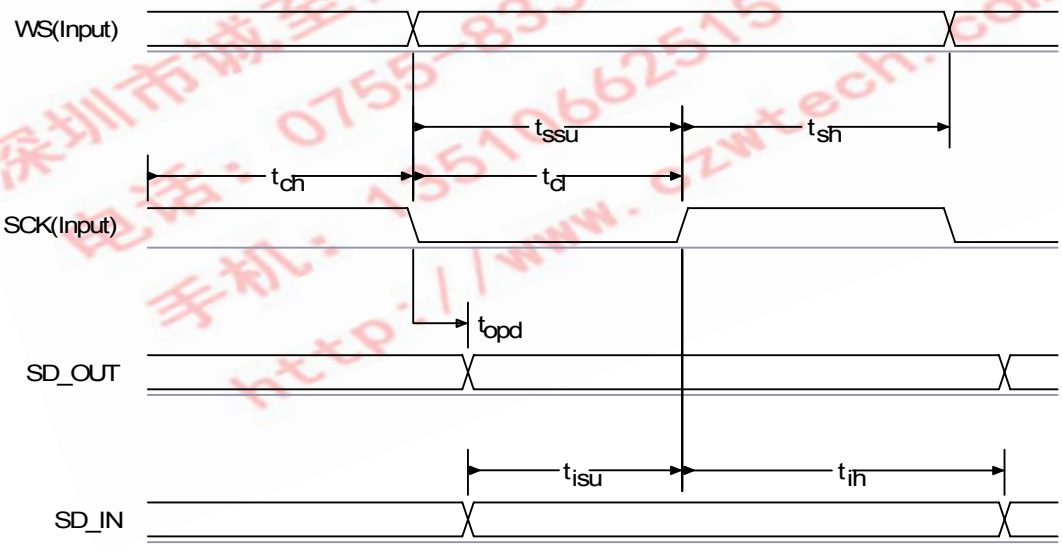


Figure 9.13: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency				
-	WS Frequency				
t_{opd}	SCK to SD_OUT delay				
t_{spd}	SCK to WS delay				
t_{isu}	SD_IN to SCK set-up time				
t_{ih}	SD_IN to SCK hold time				

Table 9.8: Digital Audio Interface Master Timing

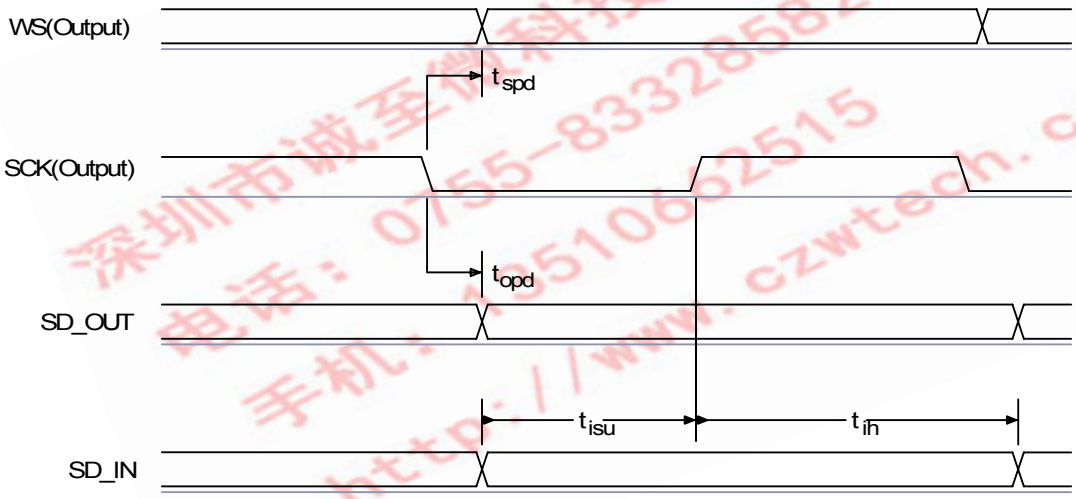


Figure 9.14: Digital Audio Interface Master Timing

10 Power Control and Regulation

10.1 Low-voltage Linear Regulator

The low-voltage linear regulator is available to power a 1.8V supply rail. Its output is connected internally to VDD_ANA, and can be connected externally to the other 1.8V power inputs.

If the low-voltage linear regulator is used a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground, should be connected to the output of the low-voltage linear regulator, VDD_ANA. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The low-voltage linear regulator is enabled by either:

- VREG_EN pin
- BlueCore4-ROM Plug-n-Go device firmware

The low-voltage linear regulator is switched into a low power mode when the device is in deep sleep mode, or in reset.

When the low-voltage linear regulator is not used the terminal VREG_IN must be left unconnected, or tied to VDD_ANA.

10.2 Power Sequencing

The 1.8V supply rails are VDD_ANA, VDD_CORE, VDD_BALUN, VDD_MEM and VDD_RADIO. CSR recommends that these supply rails are all powered at the same time.

The digital I/O supply rails are VDD_PIO, VDD_PADS and VDD_USB.

The sequence of powering the 1.8V supply rails relative to the digital I/O supply rails is not important. If the digital I/O supply rails are powered before the 1.8V supply rails, all digital I/Os will have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_BALUN and VDD_RADIO can connect directly to a 1.8V supply.

A simple RC filter is recommended for VDD_CORE and VDD_MEM to reduce transients fed back onto the power supply rails. A 2.2 ohm resistor is already provided internally for this function, but a 2.2uF cap is still needed externally. See the application schemetic to see this implementation.

The digital I/O supply rails are connected either together or independently to an appropriate voltage rail. Decoupling of the digital I/O supply rails is recommended.

10.3 External Voltage Source

If any of the supply rails for BlueCore4-ROM Plug-n-Go are supplied from an external voltage source, rather than one of the internal voltage regulators, CSR recommends that VDD_BALUN and VDD_RADIO should have less than 10mV rms noise levels between 0 and 10MHz. Also avoid single tone frequencies.

The transient response of any external regulator used should match or be better than the internal regulator available on BlueCore4-ROM Plug-n-Go. For more information, refer to regulator characteristics in Section 12. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels.

10.4 Voltage Regulator Enable Pins

The regulator enable pin, VREG_EN, enables the BlueCore4-ROM Plug-n-Go device if the on-chip regulator, Low-voltage Linear Regulator, is used.

VREG_EN pin is active high, with a logic threshold of around 1V, and a weak pull-down. It can tolerate voltages up to 4.9V, so can be connected directly to a battery to enable the device.

When the voltage regulator enable pin is pulled high the Low-voltage Linear Regulator is enabled, allowing the BlueCore4-ROM Plug-n-Go to boot-up. The firmware can then latch the regulator on and the regulator enable pin may be released.

10.5 Reset, RST#

BlueCore4-ROM Plug-n-Go can be reset from several sources:

- RST# pin
- Power-on reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RST# being active. CSR recommends that RST# be applied for a period greater than 5ms.

The power-on reset typically occurs when the VDD_CORE supply falls below 1.50V and is released when VDD_CORE rises above typically 1.60V. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are tristate. Following a reset, BlueCore4-ROM Plug-n-Go assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-ROM Plug-n-Go is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4-ROM Plug-n-Go free runs, again at a safe frequency.

10.5.1 Digital Pin States on Reset

Table 10.1 shows the pin states of BlueCore4-ROM Plug-n-Go on reset. PU and PD default to weak values unless specified otherwise.

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
USB_DP	Digital bidirectional	N/A	N/A
USB_DN	Digital bidirectional	N/A	N/A
UART_RX	Digital input with PD	PD	PD
UART_CTS	Digital input with PD	PD	PD
UART_TX	Digital bidirectional with PU	PU	PU
UART_RTS	Digital bidirectional with PU	PU	PU
SPI_MOSI	Digital input with PD	PD	PD
SPI_CLK	Digital input with PD	PD	PD
SPI_CS#	Digital input with PU	PU	PU
SPI_MISO	Digital tristate output with PD	PD	PD
PCM_IN	Digital input with PD	PD	PD

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
PCM_CLK	Digital bidirectional with PD	PD	PD
PCM_SYNC	Digital bidirectional with PD	PD	PD
PCM_OUT	Digital tristate output with PD	PD	PD
RST#	Digital input with PU	PU	PU
TEST_EN	Digital input with PD	PD	PD
PIO[15:0]	Digital bidirectional with PU/ PD	PD	PD

Table 10.1: Pin States on Reset

10.5.2 Status after Reset

The status of BlueCore4-ROM Plug-n-Go after a reset is:

- Warm reset: data rate and RAM data remain available
- Cold reset: data rate and RAM data not available

11 Application Schematic

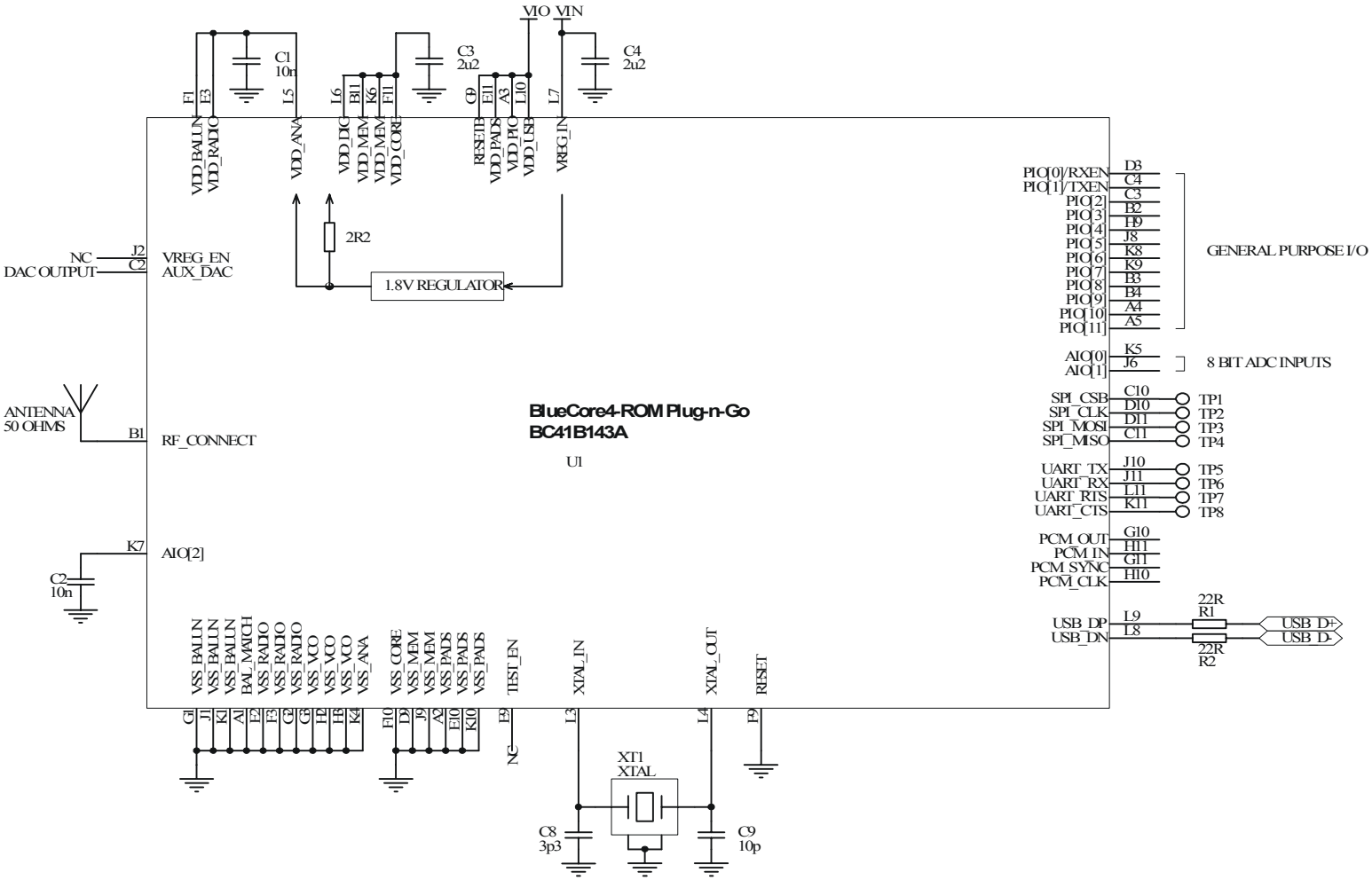


Figure 11.1: Application Circuit for Radio Characteristics Specification

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature		-40	150	°C
Core Supply Voltage	VDD_ANA, VDD_CORE, VDD_BALUN, VDD_MEM and VDD_RADIO	-0.4	2.2	V
I/O Supply Voltage	VDD_PIO, VDD_PADS and VDD_USB	-0.4	3.7	V
Supply Voltage	VREG_IN	-0.4	5.6	V
Other Terminal Voltages		VSS - 0.4	VDD + 0.4	V

12.2 Recommended Operating Conditions

Operating Condition		Min	Typ	Max	Unit
Operating Temperature Range[a]		-40	-	85	°C
Core Supply Voltage	VDD_ANA, VDD_CORE, VDD_BALUN, VDD_MEM and VDD_RADIO	1.7	1.8	1.9	V
I/O Supply Voltage	VDD_PIO, VDD_PADS and VDD_USB	1.7	3.3	3.6	V
Supply Voltage	VREG_IN	2.2	-	4.2[b]	V

[a] For radio performance over temperature refer to BlueCore4-ROM Plug-n-Go Performance Specification.

[b] BlueCore4-ROM Plug-n-Go operates up to the maximum supply voltage given in the Absolute Maximum Ratings, but RF performance is not guaranteed above 4.2V.

12.3 Input/Output Terminal Characteristics

Note:

For all I/O Terminal Characteristics:

- VDD_ANA, VDD_CORE, VDD_BALUN, VDD_MEM and VDD_RADIO at 1.8V unless shown otherwise.
- VDD_PIO, VDD_PADS and VDD_USB at 3.3V unless shown otherwise.
- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

12.3.1 Low-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.2	-	4.2	V
Output voltage (I_{load} = 70mA / VREG_IN = 3.0V)	1.70	1.78	1.85	V
Temperature coefficient	-250	0	250	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (I_{load} < 70mA)	-	-	50	mV/A
Settling time[a] [c]	-	-	50	µs
Maximum output current	70	-	-	mA
Minimum load current	5	-	-	µA
Quiescent current (excluding load, I_{load} < 1mA)	25	35	50	µA
Low Power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	4	7	10	µA
Disabled Mode [e]				
Quiescent current	1.5	2.5	3.5	nA

[a] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[b] Frequency range 100Hz to 100kHz

[c] 1mA to 115mA pulsed load

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset

[e] Regulator is disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA

12.3.2 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

12.3.3 Clocks

Clock Source	Min	Typ	Max	Unit
Crystal Oscillator				
Crystal frequency[a]	8	16	32	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω
External Clock				
Input frequency[d]	8	16	40	MHz
Clock input level[e]	0.4	-	VDD_ANA	V pk-pk
Edge jitter (allowable jitter), at zero crossing	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

[a] Integer multiple of 250kHz

[b] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[c] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF.

[d] Clock input can be any frequency between 8MHz to 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

[e] Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN.

12.3.4 Digital Terminals

Supply Voltage Levels		Min	Typ	Max	Unit
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, I_{OL} = 4.0mA	2.7V ≤ VDD ≤ 3.0V	-	-	0.2	V
	1.7V ≤ VDD ≤ 1.9V	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	2.7V ≤ VDD ≤ 3.0V	VDD - 0.2	-	-	V
	1.7V ≤ VDD ≤ 1.9V	VDD - 0.4	-	-	V
Input and Tri-state Currents					
I_i input leakage current at V_{in} = VDD or 0V		-100	0	100	nA
I_{oz} tri-state output leakage current at V_o = VDD or 0V		-100	0	100	nA
With strong pull-up		-100	-40	-10	µA
With strong pull-down		10	40	100	µA
With weak pull-up		-5	-1.0	-0.2	µA
With weak pull-down		-0.2	+1.0	5.0	µA
C_I Input Capacitance		1.0	-	5.0	pF
Resistive Strength					
R_{puw} weak pull-up strength at VDD-0.2V		500k	-	2M	Ω
R_{pdw} weak pull-down strength at 0.2V		500k	-	2M	Ω
R_{pus} strong pull-up strength at VDD-0.2V		10k	-	50k	Ω
R_{pds} strong pull-down strength at 0.2V		10k	-	50k	Ω

12.3.5 USB

	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1	-	3.6	V
Input Threshold				
V_{IL} input logic level low	-	-	0.3 x VDD_USB	V
V_{IH} input logic level high	0.7 x VDD_USB	-	-	V
Input Leakage Current				
VSS < V_{IN} < VDD_USB[a]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

[a] Internal USB pull-up disabled

12.3.6 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	8	Bits
Input voltage range[a]		0	-	VDD_ANA	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[b]		-	-	700	Samples/s

[a] LSB size = VDD_ANA/255

[b] The auxilliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

12.3.7 Auxiliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Average output step size[a]	12.5	14.5	17.0	mV
Output Voltage		monotonic[a]		
Voltage range (I_O=0mA)	VSS	-	VDD_PIO	V
Current range	-10.0	-	0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO - 0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	1	µA
Offset	-220	-	120	mV
Integral non-linearity[a]	-2	-	2	LSB
Settling time (50pF load)	-	-	10	µs

[a] Specified for an output voltage between 0.2V and VDD_PIO - 0.2V. Output is high impedance when chip is in Deep Sleep mode.

13 Product Reliability Tests for BlueCore4-ROM Plug-n-Go

The reliability tests in this section follow the tests outlined in the AEC-Q100 and were performed on BlueCore4-ROM Plug-n-Go in LFBGA 96-Ball 10 x 10 x 1.6mm 0.8mm pitch I/O (lead-free solder balls). Samples are electrically tested at ambient temperature.

This package qualification will (where moisture sensitivity preconditioning is required) use IPC/JEDEC MSL3, i.e. the finished product is allowed a maximum exposure to a 30°C/60% RH environment for 168 hours before mounting.

As part of CSR's automotive test program, customers will have access to the initial device reliability test report. They will also have access to a quarterly reliability test report update for automotive parts.

13.1 Automotive Die Test for BC41B43A-ANN-E4

Test	Test Conditions	Specification	Sample Size
ESD	Human Body Model	JEDEC	24
Latch-up	Ambient	JEDEC	6
Early Life	125°C VDD_{max}	48 hours	2400
Hot Life Test	125°C VDD_{max}	1000 hours	90, 77, 77

13.2 Automotive Package Test for BC41B43A-ANN-E4

Test	Test Conditions	Specification	Sample Size
Moisture Sensitivity Preconditioning	(125°C 24 hours) 30°C / 60% RH	192 hours 3 x reflow	702
Temperature Cycling	-65ºC to 150ºC	500 cycles	231 from Precon
Highly Accelerated Stress Test (unbiased)	130ºC / 85% RH (unbiased)	96 hours	231 from Precon
Highly Accelerated Stress Test (biased)	130ºC / 85% RH VDD_{MAX}	96 hours	240 from Precon
Hot Storage	150ºC	1000 hours	231 from Precon

14 HCI Power Consumption

Operation Mode	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.43	mA
Inquiry and page scan	-	0.75	mA
ACL no traffic	Master	3.71	mA
ACL with file transfer	Master	8.44	mA
ACL no traffic	Slave	15.1	mA
ACL with file transfer	Slave	17.7	mA
ACL 40ms sniff	Master	1.58	mA
ACL 1.28s sniff	Master	0.14	mA
eSCO EV3 - Setting S1	Master	24.0	mA
SCO HV1	Master	36.3	mA
SCO HV3	Master	17.8	mA
SCO HV3 30ms sniff	Master	17.5	mA
ACL 40ms sniff	Slave	1.39	mA
ACL 1.28s sniff	Slave	0.26	mA
eSCO EV3 - Setting S1	Slave	22.7	mA
SCO HV1	Slave	35.7	mA
SCO HV3	Slave	22.7	mA
SCO HV3 30ms sniff	Slave	16.8	mA
Parked 1.28s beacon	Slave	0.19	mA
Standby Host connection[a]	-	36	µA
Reset (RST# low)[a]	-	49	µA

[a] Low-power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode. For more information about the electrical characteristics of the linear regulator, see Section 12.3.1.

Note:

Conditions: 20°C, 1.8V supply

15 CSR Green Semiconductor Products and RoHS Compliance

15.1 RoHS Statement

BlueCore4-ROM Plug-n-Go where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the *Restriction of Hazardous Substance* (RoHS).

Important Note:

There is a version of this device that contains lead (Pb) which is not RoHS compliant. See Section 17.

15.1.1 List of Restricted Materials

BlueCore4-ROM Plug-n-Go is compliant with RoHS in relation to the following substances:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- Polybrominated Biphenyl
- Polybrominated Diphenyl Ether

For further information, see CSR's *Environmental Compliance Statement for CSR RoHS Semiconductor Products.*

16 CSR Synergy and Bluetooth Software Stack

BlueCore4-ROM Plug-n-Go is supplied with Bluetooth v2.1 + EDR specification compliant stack firmware, which runs on the internal RISC MCU. The stack firmware is compatible with CSR's **Synergy™** wireless Host Software Platform, for more information see http://www.csr.com/synergy.

The BlueCore4-ROM Plug-n-Go software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC MCU and an external host processor. The upper layers of the Bluetooth stack, above the HCI, can be run either on-chip or on the host processor.

16.1 BlueCore HCI Stack

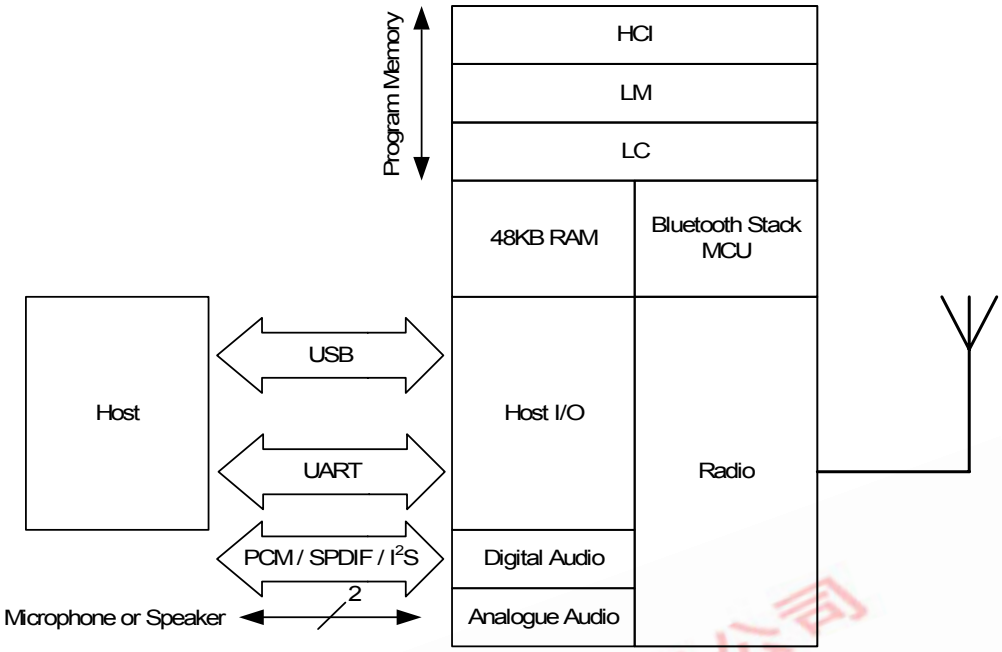


Figure 16.1: BlueCore HCI Stack

Note:

Program Memory in Figure 16.1 is internal ROM.

In the implementation shown in Figure 16.1 the internal MCU runs the Bluetooth stack up to the HCI. The Host processor must provide all upper layers including the application.

16.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v2.1 + EDR specification functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

As well as the following mandatory functions of Bluetooth v2.0 + EDR specification:

- AFH, including classifier
- Faster connection: enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

And optional Bluetooth v2.0 + EDR specification functionality:

- AFH as master and automatic channel classification
- Fast connect: interlaced inquiry and page scan plus RSSI during inquiry
- eSCO, eV3 + CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.1 + EDR specification:

- Bluetooth components:
  - Baseband including LC
  - LM
  - HCI
- Standard UART HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps
- Operation with up to 7 active slaves (this is the maximum Bluetooth v2.1 + EDR specification allows)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7
- Maximum number of simultaneous active SCO connections: 3 (BlueCore4-ROM Plug-n-Go supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.1 + EDR specification)
- Operation with up to 3 SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

16.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BCSP, a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Supports H4DS, a proprietary alternative to the standard Bluetooth UART Host Transport, supporting deep sleep for low-power applications
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BCCMD, provides:
  - Access to BlueCore4-ROM Plug-n-Go general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of BlueCore4-ROM Plug-n-Go external pins. This is normally used to build a battery monitor
- A block of BCCMD commands provides access to the BlueCore4-ROM Plug-n-Go persistent store configuration database . The database sets the BlueCore4-ROM Plug-n-Go Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, LM, etc.
- A UART break condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the IC in a low power state, preventing normal initialisation while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a deep sleep state.)
- A block of Bluetooth radio test or BIST commands allows direct control of the BlueCore4-ROM Plug-n-Go radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the PCM interface (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

17 Ordering Information

Interface Version	Package			Order Number	RoHS Compliant
	Type	Size	Shipment Method		
UART and USB	LFBGA 96-Ball (Pb free)	10 x 10 x 1.6mm, 0.8mm pitch	Tape and reel	BC41B143Axx-ANN-E4[a]	Yes
UART and USB	LFBGA 96-Ball (Contains Pb)	10 x 10 x 1.6mm, 0.8mm pitch	Tape and reel	BC41B143Axx-ABN-E4[a]	No

[a] BlueCore4-ROM Plug-n-Go is a ROM-based device where the product code has the form BC41B143Axx. xx is the specific ROM-variant, 07 is the ROM-variant for BC41B143A07-ANN-E4.

Note:

Minimum Order Quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts

17.1 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

18 Document References

Document	Reference, Date
BlueCore4-ROM Plug-n-Go Performance Specification	CS-122089-SP
Bluetooth and IEEE 802.11 b/g Coexistence Solutions Overview	bcore-an-066P
Bluetooth and USB Design Considerations	CS-101412-AN
Core Specification of the Bluetooth System	v2.1 + EDR, 26 July 2007
Environmental Compliance Statement for CSR RoHS Semiconductor Products	CB-001021-ST
IC Packing and Labelling Specification	CS-112584-SPP
Selection of I^2C EEPROMS for Use with BlueCore	bcore-an-008P
Test Suite Structure (TSS) and Test Purposes (TP) System Specification 1.2/2.0/2.0 + EDR/ 2.1/2.1 + EDR	RF.TS/2.1.E.0, 27 December 2006
Typical Solder Reflow Profile for Lead-free Devices Information Note	CS-116434-AN
Universal Serial Bus Specification	v2.0, 27 April 2000

Terms and Definitions

Term	Definition
3G	3rd Generation of mobile communications technology
8DPSK	8-phase Differential Phase Shift Keying
π/4 DQPSK	π/4 rotated Differential Quaternary Phase Shift Keying
μ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
AC	Alternating Current
ACK	ACKnowledge
ACL	Asynchronous Connection-oriented
ADC	Analogue to Digital Converter
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIO	Analogue Input/Output
BCCMD	BlueCore Command
BCSP	BlueCore Serial Protocol
BIST	Built-In Self-Test
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
codec	Coder decoder
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DC	Direct Current
DDS	Direct Digital Synthesis
DFU	Device Firmware Upgrade
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
etc	*et cetera*, and the rest, and so forth
FHS	Frequency Hop Synchronisation
FSK	Frequency Shift Keying
GCI	General Circuit Interface
GFSK	Gaussian Frequency Shift Keying
GSM	Global System for Mobile communications
H4DS	H4 Deep Sleep
HCI	Host Controller Interface

Term	Definition
I^2C	Inter-Integrated Circuit Interface
I^2S	Inter-Integrated Circuit Sound
i.e.	*Id est*, that is
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
IQ	In-Phase and Quadrature
ISDN	Integrated Services Digital Network
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
LC	An inductor (L) and capacitor (C) network
LC	Link Controller
LCD	Liquid-Crystal Display
LM	Link Manager
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LSB	Least-Significant Bit (or Byte)
Mb	Megabit
Mbps	Megabits per second
MCU	MicroController Unit
MISO	Master In Slave Out
MMU	Memory Management Unit
MSB	Most Significant Bit (or Byte)
N/A	Not Applicable
NC	Not Connect
NSMD	Non Solder Mask Defined
OHCI	Open Host Controller Interface
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Pull-down
PIO	Programmable Input/Output
ppm	parts per million
PS Key	Persistent Store Key
PU	Pull-up
RAM	Random Access Memory
RC	Resistor Capacitor
RF	Radio Frequency
RH	Relative Humidity
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory

Term	Definition
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented
SIG	(Bluetooth) Special Interest Group
SPI	Serial Peripheral Interface
TBD	To Be Defined
TCXO	Temperature Compensated crystal Oscillator
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHCI	Upper Host Control Interface
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network